WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a duty cycle correction (DCC) circuit that receives first and second clock signals and outputs a duty cycle adjusted clock signal; and

a control circuit that detects a process variation and controls respective slew rates of the first and second clock signals based on the detected process variation.

2. The device of claim 1, wherein the DCC circuit comprises:

a first inverter having an input that receives the first clock signal;

a second inverter having an input that receives the second clock signal;

a third inverter having an input commonly connected to outputs of the first and second inverters;

a first variable capacitor connected between the input of the first inverter and a ground voltage; and

a second variable capacitor connected between the input of the first inverter and the ground voltage,

wherein respective capacitance values of the first and second variable capacitors are set by the control circuit.

3. The device of claim 2, wherein the control circuit comprises:

a process variation detector that detects the process variation and outputs a voltage signal corresponding to the process variation;

a differential amplifier that receives the signal output from the process variation detector and a reference signal, and amplifies a difference between the voltage signal and the reference signal; and

an analog-to-digital converter (ADC) that converts a signal output from the differential amplifier into a digital signal,

wherein the digital signal output from the ADC is a control signal for controlling the capacitance values of the first and second capacitors.

4. The device of claim 3, wherein the process variation detector comprises a plurality of series connected PMOS transistors that have gates

connected to a ground voltage, and wherein the output signal of the process variation detector is dependent upon the process variation.

5. The device of claim 3, wherein the process variation detector comprises a plurality of series connected NMOS transistors that have gates connected to a reference supply voltage, and wherein the output signal of the process variation detector is dependent upon the process variation.

6. The device of claim 1, wherein a phase of the first clock signal is opposite to a phase of the second clock signal.

7. The device of claim 1, further comprising an amplifying circuit that receives an external clock signal and outputs the first and second clock signals corresponding to the external clock.

8. The device of claim 1, wherein the duty cycle adjusted clock signal is an internal clock signal of a synchronous semiconductor memory device.

9. The device of claim 8, wherein the synchronous semiconductor memory device is a double data rate (DDR) synchronous semiconductor memory device.

10. A synchronous semiconductor memory device comprising:

a first inverter having an input that receives a first clock signal;

a second inverter having an input that receives a second clock signal which is opposite in phase to the first clock signal;

a third inverter having an input commonly connected to outputs of the first and second inverters;

a first capacitor unit having a plurality of capacitors that are selectively connected between the input of the first inverter and a ground voltage to define a first capacitance value between the first inverter and the ground voltage;

a second capacitor unit having a plurality of capacitors that are selectively connected between the input of the second inverter and the ground voltage to define

a second capacitance value between the second inverter and the ground voltage; and

a control circuit that detects a process variation and controls respective slew rates of the first and second clock signals based on the detected process variation,

wherein the control circuit controls the respective slew rates of the first and second clock signals by adjusting the first and second capacitance values of the first and second capacitor units, respectively.

11. The device of claim 10, wherein the control circuit comprises:

a process variation detector that detects the process variation and outputs a voltage signal corresponding to the process variation;

a differential amplifier that receives the signal output from the process variation detector and a reference signal, and amplifies a difference between the voltage signal and the reference signal; and

an analog-to-digital converter (ADC) that converts a signal output from the differential amplifier into a digital signal,

wherein the digital signal output from the ADC is a control signal for controlling the first and capacitance values of the first and second capacitor units, respectively.

12. The device of claim 10, wherein the duty cycle adjusted clock signal is an internal clock signal of a synchronous semiconductor memory device.

13. The device of claim 12, wherein the synchronous semiconductor memory device is a double data rate (DDR) synchronous semiconductor memory device.